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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,928	10/22/2003	Dong-Ho Han	P16829	6901

28062 7590 08/21/2006

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/690,928	HAN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7,29-32 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,7,29-32 and 36-38* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 6-7, 29-32, and 36-38 are rejected under 35 U.S.C. 103(a) as being obvious over US 6392898 to Asai et al. in view of US 6373719 to Behling et al. or US 6068782 to Brandt et al.

Regarding claim 6, Asai discloses an apparatus in fig.1 comprising: a substrate 30, col. 8 line 38, a pair of signal traces 34U, col. 6 line 13, formed directly on the substrate 30 and spaced from each other; a filler material 40, fig. 4(E) col. 8 line 57, directly on the substrate 30 and between the signal traces 43a/44a, the filler material 40

having a dielectric constant, and a solder mask layer 44, fig. 4(G), col. 9 line 57, directly on the signal traces 34U and directly on the filler material 40, fig. 4(G), wherein the filler material 40 has a height that is substantially equal to a height of the signal traces 34U, fig. 4(F).

But, Asai does not expressly discloses the dielectric constant of the filler material 40 that is higher than a dielectric constant of the substrate 30 and the solder mask 44.

However, Behling discloses an apparatus in fig. 4 comprising a wiring board substrate 32, col. 5 line 32, a pair of signal traces 34/36, col. 5 line 35, formed directly on the substrate 32 and spaced from each other, fig. 2; a filler material 40, col. 5 line 39, directly on the substrate 32 and between the signal traces 34/36, the filler material 40 having a dielectric constant higher than a dielectric constant of the substrate 32. The material 40 includes ceramic (dielectric larger than 100) and various polymers including polyurethane (PU) (dielectric about 6) or fluoro and chlorofluoro polymer, col. 5 line 45 and col. 6 lines 8-10 that would have dielectric constant higher than the dielectric of wiring glass epoxy resin board (dielectric about 4) and solder resist material (dielectric about 4 or less). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric material between signal traces teaching of Behling with Asai's device, because it would have provided over voltage protection as taught by Behling, see abstract. Furthermore, Brandt discloses the capacitor dielectric can be polymer including PU, ceramic, PVDF,

and others, col. 4 lines 18-25. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric material teaching of Behling and Brandt with Asai's device for intended purpose, MPEP 2144.07, and/or to increase the capacitance of the structure.

Regarding claim 7, Asai does not disclose the apparatus wherein the filler material 40 has a dielectric constant in excess of 4.

However, Behling discloses the apparatus wherein the filler material 40 has a dielectric constant in excess of 4 for the same reasons as discussed in claim 6.

Regarding claim 29, Asai does not disclose the filler material 45a has a height that is substantially equal to a height of the signal traces and filler material includes polyvinylidene diflouride (PVDF).

However, Brandt discloses an apparatus wherein the filler material 120 has a height that is substantially equal to the height of the signal line 190, fig. 6. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Brandt with Williams's device to create different configuration of embedded capacitor for indented used, MPEP 2144.07.

Regarding claim 30, Asai discloses the apparatus wherein a metal ground plane 34D, fig. 1 col. 8 line 42, on an opposite side of the substrate 30 from the signal traces, fig. 1.

Regarding claim 31, Asai discloses an apparatus in fig. 1 comprising: a substrate 30, fig. 1, a pair of signal traces 34U formed on the substrate 30 and spaced from each

other, fig. 4(E); a filler material 40 on the substrate 30 and between the signal traces 34U, the filler material having a dielectric constant; and a metal ground plane 34D on an opposite side of the substrate 30 from the signal traces 34U, fig. 1; wherein the filler material 40 has a height that is substantially equal to a height of the signal traces 34U.

But, Asai does not expressly discloses the dielectric constant of the filler material 40 that is higher than a dielectric constant of the substrate 30 and the solder mask 44.

However, Behling discloses an apparatus in fig. 4 comprising a wiring board substrate 32, col. 5 line 32, a pair of signal traces 34/36, col. 5 line 35, formed directly on the substrate 32 and spaced from each other, fig. 2; a filler material 40, col. 5 line 39, directly on the substrate 32 and between the signal traces 34/36, the filler material 40 having a dielectric constant higher than a dielectric constant of the substrate 32. The material 40 includes ceramic (dielectric larger than 100) and various polymers including polyurethane (PU) (dielectric about 6) or fluoro and chlorofluoro polymer, col. 5 line 45 and col. 6 lines 8-10 that would have dielectric constant higher than the dielectric of wiring glass epoxy resin board (dielectric about 4) and solder resist material (dielectric about 4 or less). At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric material between signal traces teaching of Behling with Asai's device, because it would have provided over voltage protection as taught by Behling, see abstract. Furthermore, Brandt discloses the capacitor dielectric can be polymer including PU, ceramic, PVDF,

and others, col. 4 lines 18-25. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric material teaching of Behling and Brandt with Asai's device for intended purpose, MPEP 2144.07.

Regarding claim 32, Asai discloses the apparatus wherein: the signal traces 34U are formed directly on the substrate 30, fig. 1; the filler material 40 is directly in contact with the substrate 30; and the ground plane 34D is directly in contact with the substrate 30, fig. 1.

Regarding claim 36, Asai discloses the apparatus wherein the substrate 30 includes a resin, in which fibers are embedded, col. 8 line 38.

But Asai does not disclose the dielectric constant of the filler material 40 being higher than a dielectric constant of the resin.

However, Behling discloses the apparatus wherein the substrate 32 includes a resin, in which fibers are embedded, col. 5 lines 32-34, and the dielectric constant of the filler material 40 being higher than a dielectric constant of the resin for the same reasons as discussed in claim 6.

Regarding claims 37-38, Asai discloses the apparatus wherein the signal traces are formed of copper, col. 8 line 42, wherein the filler material 40 substantially fills a space between the signal traces 34U, fig. 1.

Response to Arguments

4. Applicant's arguments filed 16 July 2006 have been fully considered but they are not persuasive.

a. The Applicant argues that traces 34D/34U of Asai are "ground layer", not signal traces, while layer 34/34 of Behling are "ground bar", not signal lines. This is not persuasive because Asai a portion 34U is being as "ground layer", while other portion is being used as "signal trace" connecting to IC 80 as shown in fig. 12, while Behling discloses the trace 34 is connected to a I/O of one or more chip, col. 3 line 63-65. Furthermore, the term "signal traces' is being interpreted as "a electrically conductive material".

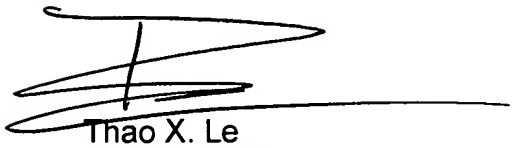
b. The Applicant argues that neither Asai nor Behling has nothing to do with the present application, which is concerned with improving the performance of differential signal traces. The Examiner respectfully disagrees because it is not necessary in order to establish a prima facie case of obviousness... that there be a suggestion or expectation from the prior art that the claimed invention will have the same or a similar utility as one newly discovered by the applicant *In re Dillon*, 919 F.2d at 692, 16 USPQ2d at 1900. Thus, it is not necessary that the prior art suggest the combination to achieve the same advantage or results discovered by applicant. See MPEP § 2144.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
16 Aug. 2006